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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/691,501	10/24/2003	David Walter Flynn	550-466	7230

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EXAMINER	
DINH, NGOC V	

ART UNIT	PAPER NUMBER
2189	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/691,501	FLYNN ET AL.	
	Examiner	Art Unit	
	NGOC V. DINH	2189	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 November 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

FINAL REJECTION

1. This Office Action is responsive to Appeal Brief filed 11/02/07.

In view of the appeal brief filed on 11/02/2007, PROSECUTION IS HEREBY REOPENED. New grounds of rejection are set forth below.

To avoid abandonment of the application, appellant must exercise one of the following two options:(1) file a reply under 37 CFR 1.111 (if this Office action is non-final) or a reply under 37 CFR 1.113 (if this Office action is final); or,(2) initiate a new appeal by filing a notice of appeal under 37 CFR 41.31 followed by an appeal brief under 37 CFR 41.37. The previously paid notice of appeal fee and appeal brief fee can be applied to the new appeal. If, however, the appeal fees set forth in 37 CFR 41.20 have been increased since they were previously paid, then appellant must pay the difference between the increased fees and the amount previously paid.

A Supervisory Patent Examiner (SPE) has approved of reopening prosecution by signing at the end of the office action.

The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

2. Applicant's arguments have been fully considered but are not persuasive. In the remarks, applicants argue in substance that:

a) "Godfrey's system bus 100 is not coupled to the memory 100".

The Examiner respectfully submits that applicant's position is misplaced:

The SCAN_PATH is part of the system bus 100 [the configuration scan data from each peripheral device is sequentially shifted out of each configuration register into external memory 200 via SCAN_PATH, col. 4/65 to col. 5/2; Likewise, the external memory 200 is coupled to the input pin IN, so that configuration scan data from external memory 200 can be synchronously shifted into each peripheral configuration register via SCAN_PATH, col. 5/3-6].

It's clearly, as mentioned above that the configuration data is shifted in and out between the entire bus 100 and SCAN_PATH. Since the Applicant is most knowledgeable of the present invention and prior art, the Examiner would like to call Applicant's attention that all scan data in

each configuration register as a result of the JTAG self test/diagnosis must have a path which is connected to the external memory so that the scan data of each register can be saved into external memory, or the configuration data can be loaded into each register from the external memory as taught by Godfrey [col. 6/45-50]. Godfrey further teaches [**the scan path is in accordance with IEEE 1149.1 bus standard**, col. 10/claim 15]. If the bus 100 of Godfrey is not connected to memory 200, then the save/restore operation of Godfrey's system is meaningless.

b) Godfrey's system bus 100 is not a Multi-Bit wide system bus. The examiner agrees with the applicant that Godfrey does not use multi-bit wide system bus for transfer state information. However, multi-bit wide system bus is well-known in the prior art for its fast transferring speed. To clarify that the prior art teaches the method of save/restore registers' status information using multi-bit bus system, the examiner cites reference Nishimura et al. PN. 6,223,279 that teaches save/restore registers' status information using multi-bit bus system [Nishimura, 16 bit/64 bit, wide bandwidth bus, col. 8/30-35; col. 10/30-35; col. 11/45-50].

The rest of the dependent claims are not patentable. All dependent claims describe a well-known self test feature in the prior art: the Joint Test Access group (JTAG). In the 1980s, The Institute of Electrical and Electronic Engineers (IEEE), in fact, organized the so-called Joint Test Action Group ("JTAG") which, in 1990, published IEEE Standard 1149.1 relating to a so-called "boundary-scan architecture" (hereafter "JTAG Standard" or "JTAG architecture").
The JTAG architecture isolates faults at the external level of the core logic by locating a "boundary-scan cell" (BSC) at each of the device's I/O pads, i.e. around the device's boundary. The boundary-scan cells are connected together to form a relatively long "Boundary-Scan Register" that may be loaded through a Test Data Input (TDI) and unloaded through a Test Data Output (TDO). The JTAG architecture beneficially allows for fault isolation by permitting the signals at all I/O pads of one or more devices to be observed, or loaded with desired values, or both.
In a computer system, typical peripheral devices include state registers, instruction registers, status and data registers. Certain registers store configuration information needed for the peripheral devices' proper operation during start up. On system start up, the execution unit

initializes each peripheral device with device specific initial configuration data. This initialization could occur during a cold start-up, or after a system crash. During a standby or sleep state, the power supplied to the peripheral devices being cut off, information held in the registers may be lost. Thus, before the system is placed into standby or sleep state, the information in each registers must be saved into a non-volatile memory, such that when the system is placed into operation state, the information stored in the non-volatile memory of each of the register can be re-loaded back into those registers. In the 1980s, the JTAG test device is developed to perform a boundary scan test for testing micro-controller peripheral boundary scan cell registers in order to save/restore scan information of state devices.

Accordingly, applicant's arguments are moot in view of new ground(s) rejection.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-2, 13-14 are rejected under 35 U.S.C.102 (b) as being anticipated by Nishimura et al. PN 6,223,279.

Claims 1-2 and 13-14, Nishimura teaches apparatus for processing data [fig. 3-4], comprising: a circuit used in processing data [fig. 23-4], said circuit having one or more nodes [register sets RF1-RF8, fig. 2; col. 2/20-30; RF0-RF1, fig. 9; col. 10/14-30] for storing one or more data values that together define a state of said circuit [content of general purpose register, col. 2/53-60];
a memory for storing data [RAM, ROM, col. 2/12-15];
a multi-bit wide system bus [16/64 bit bus, col. 8/22-30; col. 4/40-46]; and

a state saving controller [control 27, fig. 5; col. 7/52-55] coupled to said circuit and said system bus and operable in response to a state saving trigger [interrupt, col. 8/48-55] to read said data values defining a state of said circuit from said one or more nodes and to generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said memory such that said state of said circuit is restorable using said one or more state saving multi-bit data words [col. 4/24-45; col. 6/37-60; col. 7/50-65; col. 8/22-55; col. 9/34-50; col. 10/30-65].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-7, 9, 11-12-19, 21, 23-24 are rejected under 35 U.S.C 103(a) as being unpatentable over Godfrey PN. 6,550,031, and in view of Nishimura PN. 6,223,279.

Claims 1, 13: Godfrey teaches apparatus for processing data [microcontroller, col. 3, lines 25-30; fig. 1], comprising:

a circuit used in processing data [fig. 2, col. 4, lines 48-65], said circuit having one or more nodes [peripheral registers, 104a-b, 120a-b, 108a-b, ... fig. 2; plurality of miscellaneous logic, col. 9, claim 1] for storing one or more data values that together define a state of said circuit [col. 1, lines 55-62; configuration state of peripheral, col. 5, lines 8-25];

a memory for storing data 200, fig. 2];

a system bus [bus 100, fig. 2; bus 100 connected to memory 200 via scan-path, col. 5, lines 8-10, 27-35; fig. 3] coupled to said circuit and said memory and operable to transfer multi-bit data words between said circuit and said memory in response to memory transfer requests issued upon said system bus during normal processing operation of said circuit and said memory [col. 3, line 65 to col.4, line 5]; and

a state saving controller [trigger, a trigger can be used to capture the data of the miscellaneous logic into scan cells, col. 3, lines 11-20; col. 8, lines 29-40] coupled to said circuit and said system bus and operable in response to a state saving trigger to read said data values defining a state of said circuit from said one or more nodes [col. 8, lines 54-60] and to generate a sequence of memory write requests on said system bus that write one or more state saving multi-bit data words representing said data values into said memory such that said state of said circuit is restorable using said one or more state saving multi-bit data words [col. 1, lines 55-65; SAVE/RESTORE col. 3, lines 50-60; col. 6, lines 30-40; col. 9, lines 12-35].

Godfrey does not teach system bus is a multi-bit wide system bus.
Nishimura teaches a method of save/restore state devices utilizing multi-bit wide system bus [see section 3 above].
It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine Nishimura to Godfrey so that "the content of the data memory are saved and restored at high speed" [col. 11/45-48].

Claims 2 and 14, circuit is a processor core [a core microprocessor, col. 1/30-35].

Claims 3 and 15, one or more nodes are each coupled to a respective scan chain cell [col. 2, lines 16-18, 28-32; col. 2, lines 55-65] within said circuit, said state saving controller being operable in response to said state saving trigger [col. 3, lines 11-20; col. 8, lines 29-45] to store said data values within respective scan chain cells [col. 9, scan cells, claim 1; fig. 8, trigger with scan cells] and to serially read [read out serially, col. 2, lines 20-32] said data values from said scan chain cells to form said one or more state saving multi-bit data words [col. 3, lines 37-38, fig. 5 with plural stages of scan cells for saving data; col. 2, lines 29-32, 65-67; col. 3, lines 1-5; col. 9, lines 1-10].

Claims 4 and 16, a plurality of scan chains each containing a plurality of scan chain cells, said plurality of scan chains [col. 2, lines 22-25, boundary scan chain] operating in parallel [serialization of parallel data, col. 5/20-25; col. 8/12-20 to provide respective bits that together

form a state saving multi-bit data word as said plurality of scan chains of serially read [scan hardware, col. 4/38-40; col. 2/14-32].

Claims 5 and 17, scan chain cells are also operable to perform test functions upon said circuit [JTAG test, col. 44-45; col. 9/12-25, debug system].

Claims 6 and 18, circuit is a further memory and said data values are bits of data words stored in said further memory [each element in fig. 2 is either a register or latch which stores bits of data, fig. 3; fig. 7; col. 5/27-35].

Claims 7 and 19, memory is coupled to a built-in self-test controller operable to perform self-test operations [JTAG test, col. 44-45; col. 9/12-25, debug system] upon said further memory and said state saving controller uses said built-in self-test controller to read data values from said further memory to form said state saving multi-bit data words [col. 6, lines 44-62; col. 9, lines 1-20].

Claims 9 and 21, state saving controller is operable in response to a state restoring trigger [trigger, col. 3/11-20; SAVE/RESTORE, col. 3/53-55] to generate a sequence of memory read requests [scan-read, col. 7/30-35] on said system bus that read said one or more multi-bit state saving data words from said memory via said system bus and write said data values represented by said multi-bit state saving data words to said one or more nodes to thereby **restore** [*multiple snapshots*, col. 2/62-65; *snapshots*, col. 9/ 26-28] said state of said circuit [col. 3/53-55; col. 9/13-20, debug system].

Claims 11 and 23, wherein said state saving trigger comprises execution of a state saving program instruction [col. 8, lines 29-40].

Claims 12 and 24, state saving trigger comprises initiation of a diagnostic test upon said circuit [col. 2, lines 14-29].

Claims 8 and 20, Godfrey-Nishimura does not teach data burst mode transfer.
However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further include burst mode transfer into Godfrey system to improve speed of data transmission because burst mode data transmission is a well-known method for data transfer wherein burst mode enable to transfer group of memory words as a page of data, this speed up data transfer.

5. Claims 10 and 22 are rejected under 35 U.S.C 103(a) as being unpatentable over Godfrey, in view of Nishimura, and further in view of Borden PN 5,790,561.

Claims 10 and 22, Godfrey- Nishimura does not teach multi-bit state saving data words is stored in a user specified region of said memory.
Borden teaches a boundary-scan cells test using a user register [30, fig. 2; col. 3, lines 40-45].
It would have been obvious to one having ordinary skill in the art at the time the invention was made to further include Borden's teaching into Godfrey- Nishimura's system in order to implement special user functions [col. 3, lines 45-48].

Conclusion

6. Any response to this action should be mailed to:
Under Secretary of Commerce for intellectual Property and Director of the
United States Patent and Trademark Office
PO Box 1450
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or faxed to:
(571) 273-8300, (for Official communications intended for entry).
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PMR) system. Status information for published Applications may be obtained from either Private PMR or Public PMR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http//pak-direct.uspto.gov. Should you have questions on access

to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ngoc Dinh whose telephone number is (571) 272-4191. The examiner can normally be reached on Monday-Friday 8:30 AM-5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Reginald Bragdon, can be reached on (571) 272-4204.

Ngoc Dinh
January 8, 2008

Reginald B. Bragdon

REGINALD BRAGDON
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